UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/071,373	02/08/2002	Jason M. Howard	884.584US1	1781

21186 7590 03/26/2009

SCHWEGMAN, LUNDBERG & WOESSNER, P.A.
P.O. BOX 2938
MINNEAPOLIS, MN 55402

EXAMINER	
DO, CHAT C	

ART UNIT	PAPER NUMBER
2193	

MAIL DATE	DELIVERY MODE
03/26/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte JASON M. HOWARD, YATIN V. HOSKOTE,
and SRIRAM R. VANGAL

Appeal 2008-2738
Application 10/071,373
Technology Center 2100

Decided:[1] March 26, 2009

Before LANCE LEONARD BARRY, HOWARD B. BLANKENSHIP, and ST. JOHN COURTENAY III, *Administrative Patent Judges*.

BLANKENSHIP, *Administrative Patent Judge*.

DECISION ON APPEAL

---

[1] The two-month time period for filing an appeal or commencing a civil action, as recited in 37 C.F.R. § 1.304, begins to run from the decided date shown on this page of the decision. The time period does not run from the Mail Date (paper delivery) or Notification Date (electronic delivery).

STATEMENT OF THE CASE

This is an appeal under 35 U.S.C. § 134(a) from the Examiner's final rejection of claims 8-30, which are all the claims remaining in the application. We have jurisdiction under 35 U.S.C. § 6(b).

We affirm.

Invention

Appellants claim a multiplier, capable of receiving interleaved operands, and a multi-threaded accumulator. We will discuss the terms "interleaved" and "multi-threaded" in the Analysis section, *infra*.

Representative Claims

8. An integrated circuit comprising:

a multiplier coupled to receive interleaved operands and to produce a product; and

a multi-threaded accumulator coupled to the multiplier to receive the product.

16. An accumulator circuit to accept operands from different threads interleaved in time, the accumulator having intermediate registers to simultaneously hold partial results from each of the different threads.

Prior Art

The Examiner relies on the following references as evidence of unpatentability.

Choquette US 6,480,872 B1 Nov. 12, 2002

Chip Stearns et al., *The Coreware Methodology*: Building a 200 Mflop Processor In 9 Man Months, IEEE, 549-552, (1999) ("Chip").[2]

Debabrata Ghosh et al., *A 600 MHz Half-Bit Level Pipelined Accumulator-Interleaved Multiplier Accumulator Core*, IEEE, 498-506, (1993) ("Debabrata").

Examiner's Rejections

Claims 8, 9, 15, 16, and 19-23 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Chip.

Claims 10 and 11 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Chip and Debabrata.

Claims 12-14, 17, 18, and 24-30 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Chip and Choquette.

Claim Groupings

Based on Appellants' arguments in the Appeal Brief, we will decide the appeal on the basis of independent claims 8, 16, and 23, and dependent claims 10 and 12. *See* 37 C.F.R. § 41.37(c)(1)(vii).

[2] We will follow the Examiner's convention and refer to the two non-patent references by the first names of the first-named authors.

FINDINGS OF FACT

Chip

Chip describes matrix multiplication based on an Interleaved Multiplier Accumulator algorithm, which transposes the order of the arithmetic operations to accomplish the maximum throughput. Chip at 549, col. 1, ¶ 1.

3-D graphics transformations involve 4-by-4 matrix multiplication as shown in (EQ 1) (at 549). This 3-D transformation requires a series of multiply-add operations. Traditionally, each operand cycles first through the floating-point multiplier and then through the floating-point adder. One coordinate transformation requires three passes through the floating-point adder, using the non-interleaved architecture shown in Figure 1. Chip at 550, col. 1, ¶ 3.

Chip purports that an Interleaved Multiplier-Accumulator architecture performs better than the traditional non-interleaved architecture. The floating-point multiplier and adder are pipelined to the size of the transformation matrix, and the order of the arithmetic operations is transposed. Chip at 550, col. 2, ¶ 1.

A shown in Figure 2, a 4-stage pipe exists in both the multiplier and the adder. The pipe stages allow the arithmetic cores to operate on four transformations in parallel. The floating-point multiplier and adder are effectively interleaved, with each stage transforming one coordinate on the vertex. *Id.*

Table 2 (at 552, bottom) shows how the interleaved scheme transposes the order of the operations to match the latency of the architecture. *Id.*

PRINCIPLES OF LAW -- ANTICIPATION

Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim. *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 1458 (Fed. Cir. 1984).

However, statements of mere intended use cannot serve to distinguish over an apparatus in the prior art. *See In re Schreiber*, 128 F.3d 1473, 1477 (Fed. Cir. 1997) ("It is well settled that the recitation of a new intended use for an old product does not make a claim to that old product patentable."); *In re Sinex*, 309 F.2d 488, 492 (CCPA 1962) (statement of intended use in an apparatus claim failed to distinguish over the prior art apparatus); *In re Hack*, 245 F.2d 246, 248 (CCPA 1957) ("[T]he grant of a patent on a composition or machine cannot be predicated on a new use of that machine or composition.").

ANALYSIS -- ANTICIPATION

Claims 8, 16, 23 -- § 102 over Chip

In the § 102 rejection of claim 8, the Examiner reads the "multiplier" and the "multi-threaded accumulator" on the floating point multiplier

(FMUL) and the adder (FADD), respectively, as shown in Figure 2 of Chip. (Ans. 5.)

Appellants argue that Chip's disclosure of "effectively interleaving" a multiplier and an adder is not the same as receiving actually interleaved operands at the multiplier. (Br. 8.) According to Appellants, a multiplier and adder that are "effectively interleaved," and transposing the order of the operations to match the latency of the architecture, fail to teach receiving interleaved operands. (Br. 9.)

According to the Answer (at 5 and 12), the "interleaved operands" are operands "*a, e, i, m*" input into FMUL as shown in Figure 2 of Chip, which are each multiplied with operand "x" as shown in the four FMUL stages (Fig. 2) and in Table 2. The Examiner's finding appears to represent a shift in position. (*Cf.* Final Rejection at 9, top).

Appellants also argue that Chip does not describe a "multi-threaded accumulator" as required by claim 8. Chip at Table 2 shows where "ax + by" is performed in an adder operation. Thus, any operations including x and y are combined in the adder of Chip and cannot be multi-threads, according to Appellants. (Br. 9-10.)

Appellants' disclosure indicates that data in input streams that alternate in time are "interleaved" (*see* Spec. 3:11-12), as exemplified by X and Y input streams in the table at the bottom of page 4 of the Specification. Appellants' disclosure also indicates that an accumulator is "multi-threaded" because it operates on at least two "threads" simultaneously. In the example

shown in the table at page 4 of the Specification, one thread is represented by X_j and the other thread is represented by Y_j. The table demonstrates multi-threading because operations on the X and Y data streams are maintained separately. (*See* Spec. 5:1-10; *see also* Br. 10, top.) The Examiner does not appear to offer any definitions for "interleaved" and "multi-threaded" that differ from those suggested by Appellants in the Specification and Appeal Brief. We thus presume that Appellants' indications for the terms "interleaved" and "multi-threaded" in the Specification are consistent with the artisan's understanding.

Chip at page 552, Table 2, shows that adder operations with respect to the "a, e, i, and m" operands are maintained separately, even though multiplied by the "x" operand, as shown in the "Adder Operation" columns and as shown in the Examiner's "extended" table at page 13 of the Answer.

Contrary to Appellants' indication at the bottom of page 8 of the Appeal Brief, instant claim 8 does not require receiving "actually interleaved operands" at the multiplier. Claim 8 recites a multiplier "coupled to receive" interleaved operands "and to produce a product." The "multi-threaded accumulator" is "coupled" to the multiplier "to receive the product." The claim does not specify what operands might be used to produce "the product" that the accumulator is "coupled to receive." The "coupled to" language of the claim results in a claim that does not require multiplying by the multiplier, nor reception of a product by the accumulator. Nor, for that matter, does the claim require that the accumulator accumulate anything.

In our estimation, the Examiner has shown that the multiplier in Chip is at least "coupled to receive" interleaved operands, whether or not the particular operands "a, e, i, and m" might themselves be regarded as interleaved operands.

Further, we see no reason why the accumulator in Chip cannot be considered "multi-threaded," in view the Examiner's findings in the Answer (e.g., the "a, e, i, and m" operands being maintained separately). Appellants chose not to a file a Reply Brief in response to the Answer, which might have attempted to demonstrate error in the Examiner's apparently new reading of the claim on Chip.

On the record before us, we are not persuaded of error in the Examiner's finding of anticipation with respect to claim 18. We sustain the rejection of claim 18 over Chip.

With respect to claims 16 and 23, Appellants point out that Chip discloses that the pipe stages (Fig. 2) allow the arithmetic cores to operate on four ordinate transformations in parallel (Chip at 550, col. 2, ¶ 1), which is shown in the four multiplier operation columns in Table 2 (*id.* at 552). However, we do not consider the disclosure of transformations in parallel to be inconsistent with the Examiner's reading of claims 16 and 23 on Chip (Ans. 5-6.)

We sustain the § 102 rejection of claims 16 and 23 over Chip, for similar reasons that we sustain the rejection of claim 8. Claim 16, in particular, has the intended-use language of "to accept" and "to

simultaneously hold" that means that the claim does not require that the accumulator circuit actually accumulate anything, and sets forth nothing different from the accumulator circuit described by Chip. Claim 23, similar to claim 8, recites a multiplier "to produce" a product, and an accumulator "coupled to receive" the product from the multiplier, which results in a claim that is broader than Appellants' arguments would suggest, and also met by the apparatus described by Chip.

PRINCIPLES OF LAW -- OBVIOUSNESS

A person having ordinary skill in the art uses known elements for their intended purpose. *Anderson's-Black Rock, Inc. v. Pavement Salvage Co.*, 396 U.S. 57 (1969) (radiant-heat burner used for its intended purpose in combination with a spreader and a tamper and screed).

"[W]hen a patent 'simply arranges old elements with each performing the same function it had been known to perform' and yields no more than one would expect from such an arrangement, the combination is obvious." *KSR Int'l Co. v. Teleflex, Inc.*, 127 S. Ct. 1727, 1740 (2007) (quoting *Sakraida v. Ag Pro, Inc.*, 425 U.S. 273, 282 (1976)).

ANALYSIS -- OBVIOUSNESS

Claim 10 -- § 103(a) over Chip and Debabrata

Claim 10 recites that the multi-threaded accumulator of base claim 8 is "configured to" sum floating point numbers having mantissas in carry-

save format. The Examiner relies on Debabrata (at 502) to teach an adder having mantissas in carry-save format.

Appellants argue (Br. 13) that Debabrata does not remedy the supposed deficiencies of Chip as applied against base claim 8, which we find to be not persuasive of error.

Appellants also argue (*id.*, 14) that a "motivation" in Debabrata, in a section of the reference on which the rejection in the Answer does not rely, is actually not a motivation. The Examiner finds (Ans. 15) that the carry-save format in well-known and conventional in the art, as evidenced by Debabrata.

Appellants have not shown that the Examiner's finding of what is conventional, which is supported by the evidence of record, to be in error. Claim 10 thus appears, at best, as the use of a known element according to it known properties that was available in the prior art.

A person having ordinary skill in the art uses known elements for their intended purpose. As the combination of claim 10 appears to represent an arrangement of old elements with nothing unexpected from the results, to one of ordinary skill in the art, we are not persuaded of error and sustain the rejection of the claim.

Claim 12 -- § 103(a) over Chip and Choquette

Claim 12 recites that a floating point conversion unit is coupled between the multiplier and the multi-threaded accumulator of base claim 8

"to convert" the product from a first floating point representation to a second floating point representation.

The Examiner relies on Choquette's teaching of a floating point conversion unit 414 (Fig. 4) coupled between a multiplier and multi-threaded accumulator as claimed. (Ans. 8.)

Appellants submit (Br. 15) that Choquette does not remedy the supposed deficiencies of Chip as applied against base claim 8, which we do not find persuasive of error in the rejection of claim 12.

Appellants also argue "there is no teaching or suggestion in the cited portion of Choquette to combine the shifter of Choquette with the matrix multiplication based on interleaved multiplier accumulator algorithm of Chip et al., as recited in the Abstract of Chip et al." (*Id.*, 16.) However, the Examiner does not allege such a specific teaching, but finds that the references would have suggested the combination. "The presence or absence of a motivation to combine references in an obviousness determination is a pure question of fact." *In re Gartside*, 203 F.3d 1305, 1316 (Fed. Cir. 2000).

Appellants also suggest that the proposed combination would be inconsistent with the interleaved Multiplier-Accumulator architecture of Chip (Br. 16), but do not provide evidence (or convincing argument) in support of the allegation.

Using a floating point conversion unit, as taught by Choquette, with the multiplier and accumulator of Chip thus appears, on this record, to be no

more than the predicable use of known elements according to their intended functions, with nothing unexpected from the combination. As the prima facie case of obviousness has not been persuasively rebutted by Appellants, we sustain the rejection of claim 12.

DECISION

The rejection of claims 8, 9, 15, 16, and 19-23 under 35 U.S.C. § 102(b) as being anticipated by Chip is affirmed.

The rejection of claims 10 and 11 under 35 U.S.C. § 103(a) as being unpatentable over Chip and Debabrata is affirmed.

The rejection of claims 12-14, 17, 18, and 24-30 under 35 U.S.C. § 103(a) as being unpatentable over Chip and Choquette is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a).

AFFIRMED

rwk

SCHWEGMAN, LUNDBERG & WOESSNER, P.A.
P.O. BOX 2938
MINNEAPOLIS MN 55402